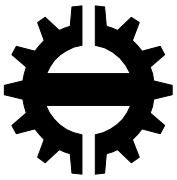

TAMPERE UNIVERSITY OF TECHNOLOGY

# D6.3.7. Demonstration of disturbance recording functions for PQ monitoring

***Final Report***

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## 1. Introduction

The OMAP-L138 C6-Integra DSP+ARM processor is selected for demonstrating IED capability for disturbance recording and PD monitoring function. The DSP used in the earlier development of PLC monitoring part was lacking processing capability and on-chip device memory. Disturbance recording function requires larger amount of data memory to record at least few seconds of disturbance event. On the other hand PD monitoring functions have need for large memory as well because of the high sampling frequency, for example, few MHz. Depending upon the algorithm, at least one complete cycle would be required to identify PD problems. Moreover, high processing power and enough memory to post-process the input signal in real-time are some of the main reason to choose the new platform.

## 2. DSP+ARM Processor

The OMAP-L138 C6-Integra™ DSP+ARM® processor is a low-power applications processor based on an ARM926EJ-S™ and a C674x DSP core. It provides significantly lower power than other members of the TMS320C6000™ platform of DSPs. The device enables OEMs and ODMs to quickly bring to market devices featuring robust operating systems support, rich user interfaces, and high processing performance life through the maximum flexibility of a fully integrated mixed processor solution. The dual-core architecture of the device provides benefits of both DSP and Reduced Instruction Set Computer (RISC) technologies, incorporating a high-performance TMS320C674x DSP core and an ARM926EJ-S core.

The device DSP core uses a two-level cache-based architecture. The Level 1 program cache (L1P) is a 32KB direct mapped cache and the Level 1 data cache (L1D) is a 32KB 2-way set-associative cache. The Level 2 program cache (L2P) consists of a 256KB memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or combinations of the two. Although the DSP L2 is accessible by ARM and other hosts in the system, an additional 128KB RAM shared memory is available for use by other hosts without affecting DSP performance.

The peripheral set includes: a 10/100 Mb/s Ethernet MAC (EMAC) with a Management Data Input/Output (MDIO) module; one USB2.0 OTG interface; one USB1.1 OHCI interface; two inter-integrated circuit (I2C) Bus interfaces; one multichannel audio serial port (McASP) with 16 serializers and FIFO buffers; two multichannel buffered serial ports (McBSP) with FIFO buffers; two SPI interfaces with multiple chip selects; four 64-bit general-purpose timers each configurable (one configurable as watchdog); a configurable 16-bit host port interface (HPI); up to 9 banks of 16 pins of general-purpose input/output (GPIO) with programmable interrupt/event generation modes, multiplexed with other peripherals; three UART interfaces (each

with RTS and CTS); two enhanced high-resolution pulse width modulator (eHRPWM) peripherals; 3 32-bit enhanced capture (eCAP) module peripherals which can be configured as 3 capture inputs or 3 auxiliary pulse width modulator (APWM) outputs; and 2 external memory interfaces: an asynchronous and SDRAM external memory interface (EMIFA) for slower memories or peripherals, and a higher speed DDR2/Mobile DDR controller.

The SATA controller provides a high-speed interface to mass data storage devices. The SATA controller supports both SATA I (1.5 Gbps) and SATA II (3.0 Gbps). The Universal Parallel Port (uPP) provides a high-speed interface to many types of data converters, FPGAs or other parallel devices.

The OMAP-L138 and C6748 processors are ideal for applications in the industrial, audio, portable medical and communications markets. The snapshot of the OMAP-L138 EVM along with User Interface (UI) board is shown in Fig. 1.

Fig. 1: OMAP-L138 EVM interfaced with UI board

## 3. Analog-to-Digital Converter

The OMAP-L138 EVM comes with UI board which is equipped with difference peripherals i.e. S-Video in/out connector, camera interface, LCD panel, Ethernet jack connector, analog-to-digital converter, digital-to-analog converter and so on. Analog-to-digital converter interfaced with UI board has been used to digitize analog signal for disturbance recorder and PD monitoring functions. The ADS901 is a high-speed pipelined analog-to-digital converter that operates from a +3V power supply. This complete converter includes a wide bandwidth track/hold and a 10-bit quantizer.

The ADS901 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for telecommunications, video and test instrumentation applications. The maximum sampling frequency of the converter is 20MHz which is quite sufficient for PD monitoring.

# 4. Universal Parallel Port (uPP)

The universal parallel port (uPP) peripheral is a multichannel, high-speed parallel interface with dedicated data lines and minimal control signals. It is designed to interface cleanly with high-speed analog-to-digital converters (ADCs) or digital-to-analog converters (DACs) with up to 16-bit data width (per channel). It may also be interconnected with field-programmable gate arrays (FPGAs) or other uPP devices to achieve high-speed digital data transfer. It can operate in receive mode, transmit mode, or duplex mode, in which its individual channels operate in opposite directions.

The uPP peripheral includes an internal DMA controller to maximize throughput and minimize CPU overhead during high-speed data transmission. All uPP transactions use the internal DMA to feed data to or retrieve data from the I/O channels. The DMA controller includes two DMA channels, which typically service separate I/O channels.

The uPP peripheral has been used to move data between A/D converter and CPU. It offers speed up to 75 MHz with 8-16 bit data width per channel. This interface makes real-time capturing and processing of data quite efficient.

# 5. Description of operation

The disturbance recorder continuously monitors the voltage level of the LV network. High speed recording is used to measure current and voltage with a sampling frequency high enough to display power system faults and transient. Disturbance recorder used today lacks the feature to monitor high frequency interference due to low sampling rate and on-chip memory. High speed recording is used to capture transient events, which are short in duration, with the recorder length typically set for one to two seconds. Recording length can also be set by the user for longer time measurement based on the available on-chip memory. Other operations of the disturbance recorder are explained below.

## 5.1. Triggering

The recording module is triggered by RMS over or under voltage. The disturbance recorder captures 7 full 50 Hz cycle and calculates RMS value for each cycle. The RMS value is compared against the upper and lower voltage threshold set based on the monitoring condition to start a

recording. Figure 2 shows the principle of recording length. Whenever the measured RMS value goes over or below the set threshold, triggering condition is met and device starts to record data of the record length which consists of pre-trigger, trigger condition and post trigger as shown in the figure given below. The device keeps recording as long as the trigger remains active.

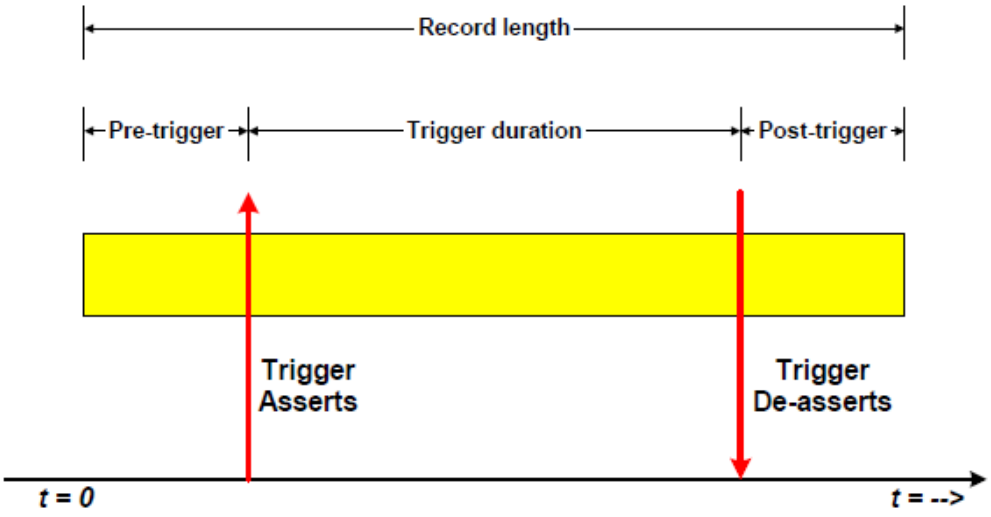


Fig. 2: Triggering method

### 5.2. Recording

When the triggering conditions are fulfilled, a recording is made the length of which are 21 full 50 Hz cycle. The recording length will be defined more precisely after testing and analyzing the records from real network and it can be adjusted according to the need of the user and applications.

## 6. Results

This section explains the results captured by the prototype of the disturbance recorder. Figure 2 shows 7 complete cycle of 50 Hz signal sampled at 18 kHz using the A/D converter interfaced with the UI board the DSP.

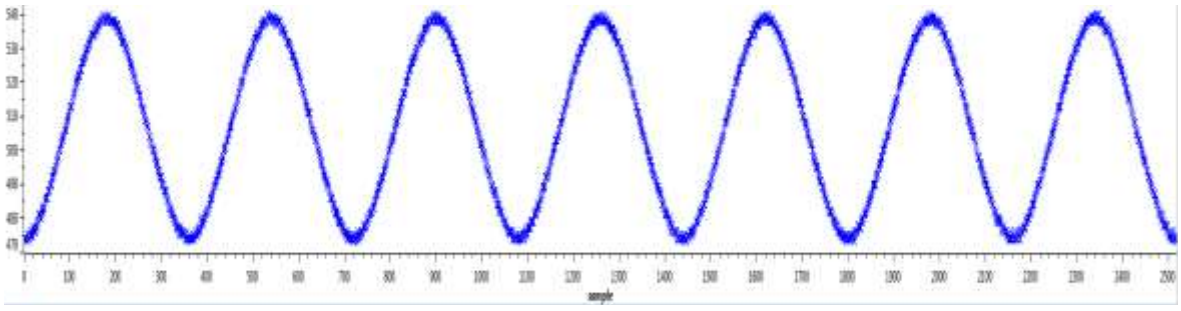

Fig. 3: Signal sampled by A/D converter

After capturing 7 full cycles, DSP computes RMS value for each cycle and compares that value against the set threshold. In this example, it was assumed that the calculated RMS value goes above or below the set threshold, recording of the event starts for a record length of 21 full 50 Hz cycles which is shown in below in Fig 4. It is evident from the graph that the record is divided into 3 sections i.e. pre-trigger, trigger duration and post-trigger. Pre-trigger corresponds to the event before the actual disturbance occurred in the network, trigger duration is the time when disturbance occurred and post-trigger is the time after triggering condition goes off. Pre-trigger and post-trigger give more information about the nature of disturbance which might be helpful to study the cause of the disturbances. The sampling is continuous throughout the recording period. The discontinuity between the pre-trigger, trigger duration and post-trigger parts of the signal as shown in Fig. 4 is due to the overlap between the parts. The final COMTRADE output waveform is reconstructed from these partly overlapping parts to form a continuous data. This diagram just demonstrates the principal that how DR will be recording the disturbances in the real network.

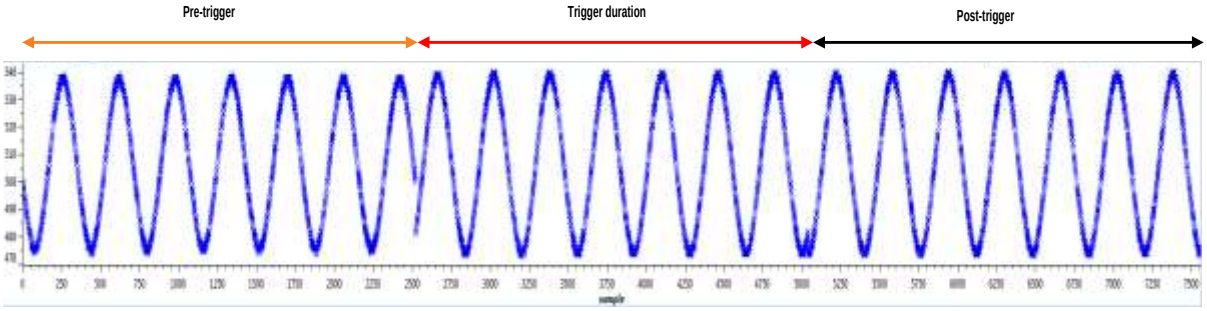


Fig. 4: Record of the event

## 7. Conclusion

The prototype of the disturbance recorder is tested in the laboratory. The uPP, high speed A/D converter and fast processing DSP have made it possible to process the data in real-time. It has shown promising results in terms of capturing and processing the signal in real-time. The device has several possibilities to store large amount of data i.e. MMC/SD card, USB and SATA interface. Any one of them will be used to capture large amount of data from the network in COMTRADE format which is a common format for the data files and exchange medium needed for the interchange of various types of faults, test and simulation data.