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Impact of strength of fault current path on the operation of decoupled double synchronous reference frame – phase locked loop

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Abstract. This paper studies the performance of decoupled double synchronous reference frame - phase locked loop (DDSRF-PLL) synchronizing method during grid fault. The study is carried out using Matlab/Simulink. The contribution of the paper is to reveal that if the DDSRF-PLL proposed in many papers is used, the control system of network side converter (NSC) may become unstable during a symmetrical grid fault. The instability problem appears only when certain tuning parameters of DDSRF-PLL are used and the fault current path is weak. Thus, the problem may not be easily detected. This paper emphasizes that it is mandatory to use PI-controller with integrator anti-windup in the loop filter of DDSRF-PLL. In addition, the impact of angular frequency limitation range on the fault ride through performance is evaluated with comparative simulations.

Key words

Wind turbine, synchronization, DDSRF-PLL, integrator anti-windup, PI-controller

1. Introduction

The amount of electricity generated using wind turbines (WT) has increased dramatically in recent years. According to World Wind Energy Association (WWEA), the worldwide WT capacity at the end of year 2011 was 239 GW covering 3 % of the world's electricity demand. [1] In the past, due to the low penetration of grid connected WTs the operation of WTs did not have great impact on the operation of the utility grid. Nowadays, the penetration level of the WTs has increased in many areas and the operation of WTs should be designed so that the stable operation of the power system is not endangered in any circumstances due to the WT connection. Thus, the power system operators have created grid codes which determine how WTs should operate under different grid conditions. [2] In order to fulfil the grid codes, WTs should be able to control its active and reactive power output as well as to stay in operation during grid disturbances.

The technical challenges above are strongly related to the control system design of the WT frequency converter. The converter consists of a generator side converter (GSC) which controls the generator speed and a network side converter (NSC) which controls the converter DC-link voltage and the reactive power output.

The most important task for WT is to generate electrical power to the network with minimized losses. This task is fulfilled when the WT feeds only fundamental frequency positive sequence currents into the network. Because the control system of the vector controlled NSC is usually realized in a synchronous reference frame, the fundamental frequency positive sequence currents can be generated if the angle of the network voltage fundamental frequency positive sequence component is somehow detected. Moreover, the currents can be divided into active and reactive current components which can be controlled independently from each other. Thus, the active and the reactive power output of the WT can be controlled as required by the grid codes.

In this study, the decoupled double synchronous reference frame – phase locked loop (DDSRF-PLL) is used to provide the angle for the control system of NSC. It is shown in this paper that the WT may become unstable during a symmetrical grid fault if the DDSRF-PLL proposed in many papers is used. [3][4][5][6] The instability problem is very harmful because it appears only when the WT with certain tuning parameters of DDSRF-PLL is connected into a weak network. Thus, the problem may not be detected. This paper underlines that it is obligatory to use PI-controller with integrator anti-windup in the loop filter (PI-controller) of DDSRF-PLL. In addition, the impact of angular frequency limitation range on the fault ride through performance is evaluated with comparative simulations.

2. DDSRF-PLL

The DDSRF-PLL consists of a decoupling network and phase locked loop operating on synchronous reference frame (SRF-PLL). The decoupling network provides positive and negative sequence components from the

input voltage vector. The synchronization to the positive sequence component of the grid voltage is achieved when the voltage positive sequence q-component is controlled to zero. This is done using SRF-PLL.

A. Decoupling network

The unbalanced grid voltage vector $\underline{u}_{\alpha\beta}$ can be expressed in stationary reference frame as follows: [5]

$$\underline{u}_{\alpha\beta} = \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = U^+ \begin{bmatrix} \cos\left(\omega t + \varphi^+\right) \\ \sin\left(\omega t + \varphi^+\right) \end{bmatrix} + U^- \begin{bmatrix} \cos\left(-\omega t + \varphi^-\right) \\ \sin\left(-\omega t + \varphi^-\right) \end{bmatrix} \tag{1}$$

where U is peak value of the phase voltage, ω is angular frequency of the grid and φ is initial angle. Superscripts + and - correspond to the positive and negative sequence references. It is assumed that the positive sequence reference frame is rotating synchronously with the fundamental frequency positive sequence grid voltage component. Thus, $\theta_{\text{sync}} = \omega t$. The positive and negative sequence components can be expressed in synchronous dq-reference frame using angle θ_{sync} which is the output of the SRF-PLL. [5]

$$\begin{aligned} \underline{u}^+_{dq} &= \begin{bmatrix} u^+_d \\ u^+_q \end{bmatrix} = \left[T^+_{dq}\right] \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \begin{bmatrix} \cos\left(\theta_{\text{sync}}\right) & \sin\left(\theta_{\text{sync}}\right) \\ -\sin\left(\theta_{\text{sync}}\right) & \cos\left(\theta_{\text{sync}}\right) \end{bmatrix} \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \\ & U^+ \begin{bmatrix} \cos\left(\varphi^+\right) \\ \sin\left(\varphi^+\right) \end{bmatrix} + U^- \cos\left(\varphi^-\right) \begin{bmatrix} \cos\left(2\omega t\right) \\ -\sin\left(2\omega t\right) \end{bmatrix} + U^- \sin\left(\varphi^-\right) \begin{bmatrix} \sin\left(2\omega t\right) \\ \cos\left(2\omega t\right) \end{bmatrix} \end{aligned} \tag{2}$$

$$\begin{aligned} \underline{u}^-_{\text{dq}} &= \begin{bmatrix} u^-_{\text{d}} \\ u^-_{\text{q}} \end{bmatrix} = \left[T^-_{\text{dq}}\right] \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \\ & U^- \begin{bmatrix} \cos\left(\varphi^-\right) \\ \sin\left(\varphi^-\right) \end{bmatrix} + U^+ \cos\left(\varphi^+\right) \begin{bmatrix} \cos\left(2\omega t\right) \\ \sin\left(2\omega t\right) \end{bmatrix} + U^+ \sin\left(\varphi^+\right) \begin{bmatrix} -\sin\left(2\omega t\right) \\ \cos\left(2\omega t\right) \end{bmatrix} \end{aligned} \tag{3}$$

The left side terms in Equations (2) and (3) are DC-values and right side terms are AC-values. The DC-values are solved in order to distinguish the positive and the negative sequence components from the grid voltage: [5]

$$\begin{aligned} & U^+ \begin{bmatrix} \cos\left(\varphi^+\right) \\ \sin\left(\varphi^+\right) \end{bmatrix} = \begin{bmatrix} U^+_{\text{d}} \\ U^+_{\text{q}} \end{bmatrix} = \\ & \begin{bmatrix} u^+_{\text{d}} \\ u^+_{\text{q}} \end{bmatrix} - U^- \cos\left(\varphi^-\right) \begin{bmatrix} \cos\left(2\omega t\right) \\ -\sin\left(2\omega t\right) \end{bmatrix} - U^- \sin\left(\varphi^-\right) \begin{bmatrix} \sin\left(2\omega t\right) \\ \cos\left(2\omega t\right) \end{bmatrix} \end{aligned} \tag{4}$$

$$\begin{aligned} & U^- \begin{bmatrix} \cos\left(\varphi^-\right) \\ \sin\left(\varphi^-\right) \end{bmatrix} = \begin{bmatrix} U^-_{\text{d}} \\ U^-_{\text{q}} \end{bmatrix} = \\ & \begin{bmatrix} u^-_{\text{d}} \\ u^-_{\text{q}} \end{bmatrix} - U^+ \cos\left(\varphi^+\right) \begin{bmatrix} \cos\left(2\omega t\right) \\ \sin\left(2\omega t\right) \end{bmatrix} - U^+ \sin\left(\varphi^+\right) \begin{bmatrix} -\sin\left(2\omega t\right) \\ \cos\left(2\omega t\right) \end{bmatrix} \end{aligned} \tag{5}$$

The decoupling network based on (4) and (5) and shown in Fig. 1 is used to cancel AC components from positive and negative sequence reference frames. The block LPF represents a simple first order low-pass filter with cut-off frequency of ω_{f}: [5]

$$LPF(s) = \frac{\omega_{\text{f}}}{s + \omega_{\text{f}}} \tag{6}$$

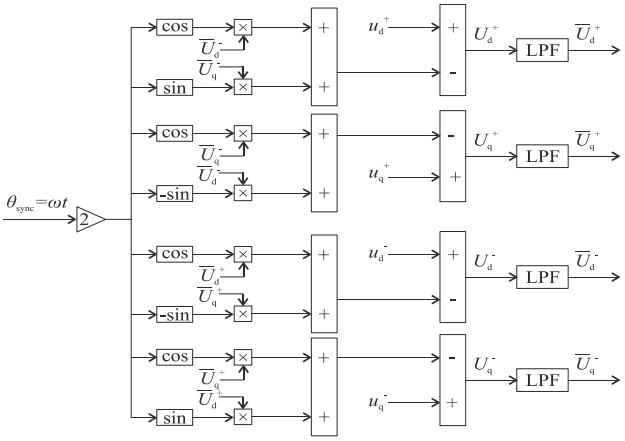

Fig. 1. Decoupling network.

The decoupling network provides positive and negative sequence components from the input voltage vector. Thus, it is possible to synchronize the control system of the NSC to the grid voltage positive sequence component which is desired in wind turbine applications. The synchronization to the positive sequence component of the grid voltage is achieved when the positive sequence q-axis voltage component U_{q}^+ is zero. In that case, the initial phase angle φ^+ is zero and the positive sequence voltage component is aligned to d^+-axis rotating with angular speed of ω. The angle of positive sequence voltage component θ_{sync} is obtained using SRF-PLL.

B. SRF-PLL

The balanced grid voltage vector in stationary reference frame can be expressed as follows: [5]

$$\underline{u}_{\alpha\beta} = \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = U \begin{bmatrix} \cos\left(\omega t\right) \\ \sin\left(\omega t\right) \end{bmatrix} \tag{7}$$

The (7) in synchronous reference frame rotating with angle provided by the synchronization system θ_{sync} is: [5]

$$\begin{bmatrix} u_{\text{d}} \\ u_{\text{q}} \end{bmatrix} = \begin{bmatrix} \cos\theta_{\text{sync}} & \sin\theta_{\text{sync}} \\ -\sin\theta_{\text{sync}} & \cos\theta_{\text{sync}} \end{bmatrix} \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = U \begin{bmatrix} \cos\left(\omega t - \theta_{\text{sync}}\right) \\ \sin\left(\omega t - \theta_{\text{sync}}\right) \end{bmatrix} \tag{8}$$

The voltage component of interest in (8) is the u_{q} since the purpose of the control system is to regulate the voltage q-component to zero. Due to the sinusoidal function in (8) the system under consideration is nonlinear. However, when the phase difference θ-θ_{sync} is small the sinusoidal term behaves almost linearly. [5] The block diagram of linearized SRF-PLL is shown in Fig. 2 and the closed loop transfer function is based on:

$$H_{\text{cl}}(s) = \frac{\theta_{\text{PLL}}}{\theta} = \frac{k_{\text{PLL}} s + \dfrac{k_{\text{PLL}}}{T_{\text{i}}}}{s^2 + k_{\text{PLL}} s + \dfrac{k_{\text{PLL}}}{T_{\text{i}}}} = \frac{2\varsigma\omega_{\text{n}} s + \omega_{\text{n}}^2}{s^2 + 2\varsigma\omega_{\text{n}} s + \omega_{\text{n}}^2} \tag{9}$$

where k_{PLL}=-U*k_{LF} represents the PLL gain, k_{LF} is loop filter gain, T_{i} is integration time, ω_{n} is undamped natural frequency and ζ is damping factor. The feed forward term ω_{ff} is used to set the frequency near the final value in order to accelerate start-up process. The angular position θ_{sync} of the rotating reference frame is attained after integration of ω_{sync}. [7]

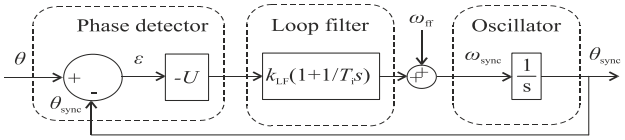

Fig. 2. Linearized block diagram of the SRF-PLL.

C. DDSRF-PLL

The DDSRF-PLL is a combination of decoupling network and SRF-PLL. The block diagram of the DDSRF-PLL is shown in Fig. 3. [3][4][5][6]

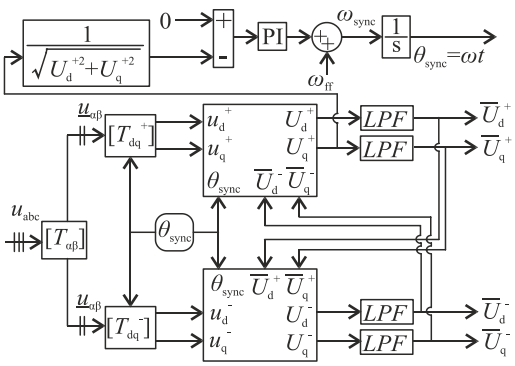

Fig. 3. The block diagram of DDSRF-PLL.

As can be seen from Fig. 2 the gain of the system depends on the loop filter parameters as well as input voltage magnitude *U*. If the input voltage drops, also the PLL gain falls down. [7] Thus, the regulated value U_q^+ is actively normalized to the amplitude of the positive sequence component of the grid voltage vector. The parameters used in DDSRF-PLL are: ω_f=2*π*50/sqrt(2), k_{LF}= -177.7, T_i= 0.0113s. The parameters are often expressed in terms of ζ and ω_n which are: ζ=sqrt(2), ω_n=2*π*20. [5][8]

D. *Frequency limitation and integrator anti-windup*

After the grid voltage dip the grid angle may change rapidly causing significant error measure ε in Fig. 2. The loop filter, which is typically a PI-controller, aims to regulate the ε to zero. As a result of the PI controller actions, the loop filter output ω_{sync} may deviate significantly from the grid voltage frequency. The consequence is increased amount of harmonics in currents fed into the network. Due to the fact that the grid frequency is a reasonably stable variable it is vice to limit the ω_{sync}. Another problem is the windup of the integrator part of the controller. [9] If the sign of significant ε remains unchanged for a reasonable time the output value of the integrator may become very large causing remarkable deviation of ω_{sync} from the grid frequency. If the ω_{sync} is limited the saturation of ω_{sync} continues for a long time due to the windup. Thus, it is important to stop the integration when the ω_{sync} saturates. This is called as integrator anti-windup and it can be realised using SRF-PLL structure shown in Fig. 4.

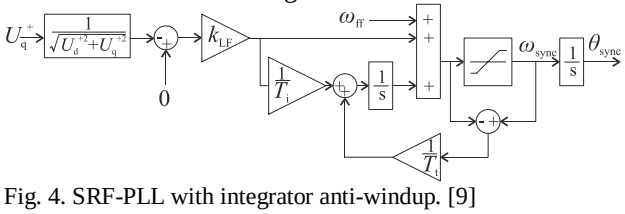

Fig. 4. SRF-PLL with integrator anti-windup. [9]

Generally, the anti-windup tracking time constant T_t should be small enough to prevent the integrator from saturation. However, very small value of T_t increases the anti-windup gain significantly which decreases the effect of the loop filter integral controller. Thus, the performance of the loop filter may decrease. In [9], it is suggested that the T_t should be smaller than T_i.

3. Simulation model

The network model used in the study is shown in Fig. 5. The 110 kV transmission network consists of two parallel feeders. The feeder 1 represents weak feeder having much greater impedance compared to feeder 2. The feeder 1 impedance values including transformer TF1 are chosen so that when circuit breakers Cb_{f21} and Cb_{f22} are opened the feeder impedance equals to the impedance found in real Finnish network. The feeder 2 impedances have been similarly measured from the real Finnish grid.

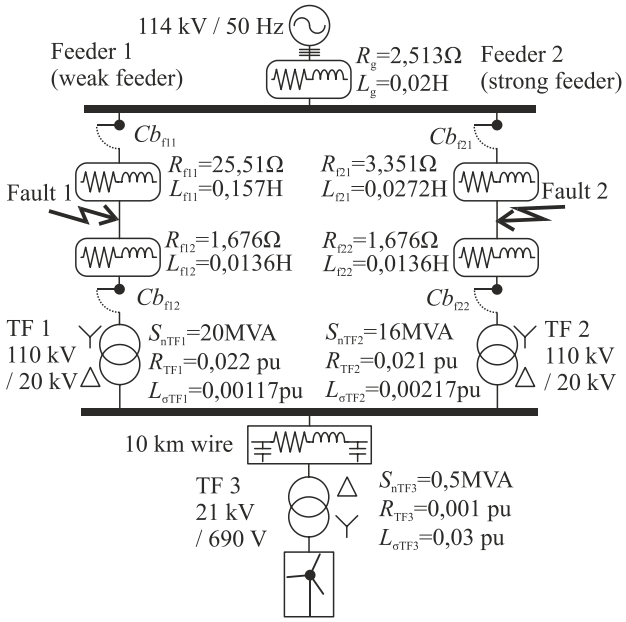

Fig. 5. Network model with used parameters.

The wind turbine system model including the control system of the NSC is shown in Fig. 6. The target of this study is to analyse the synchronization of the WT system. Hence, it is unnecessary to model the mechanical parts of the WT in detail because the mechanical time constants are much greater than time constants related to synchronization. Thus, the mechanical parts, generator and GSC are modelled as a current source i_{WT} in the DC-link of the frequency converter where the generated electrical power p_{gen} is controllable. The value for i_{WT} is calculated from:

$$i_{WT} = \frac{p_{gen}}{u_{dc}} \tag{10}$$

where u_{dc} is the DC-link voltage. The braking chopper for DC-link overvoltage protection is modelled in the DC-link of the frequency converter. The switch activating the chopper is closed when the DC-link voltage increases above 1250V and the surplus energy is dissipated in the resistance R_{dc}.

The vector control of NSC is done in the reference frame synchronized to the connection point voltage $\underline{u}_{sync}$ using DDSRF-PLL. The phase angle of the fundamental frequency component of the voltage is the output of the block *Sync*. The aim of the dc-link voltage controller is to maintain constant dc-link voltage, thereby ensuring that the generated active power p_{gen} in (10) is fed into the network. The output of the dc-link voltage controller is the d-component of the converter current i_{L1d}. Reactive power controller outputs the reference of q-axis component of the grid side current $i_{L1,q}^*$. The reference value for the connection point instantaneous reactive power q^* is zero in the study. During a voltage dip, the reference for i_{L1q}^* depends on the network voltage magnitude $|\underline{u}_{sync}|$. If the voltage is lower than nominal value, reactive power is injected to the network to support the network voltage. The calculation of instantaneous reactive power q is performed in the *pq-calculation* block. The reference currents i_{L1d}^* and i_{L1q}^* are compared to the measured values and the errors are fed to the current controllers. The outputs of the current controllers are the voltage components over LCL-filter inductors u_{Ld}^* and u_{Lq}^*. Removing the cross-coupling terms and with the help of the measured connection point voltage components $u_{sync,d}$ and $u_{sync,q}$, the NSC voltage reference components $u_{conv,d}^*$ and $u_{conv,q}^*$ can be calculated.

The switching action is not taken into account in this study and the NSC is assumed to produce the reference voltage $\underline{u}_{NSC}$ ideally. However, the design of the LCL-filter was based on the switching frequency f_{sw} of 3.6 kHz. The resonance frequency of the filter f_{res} is 1072 Hz when the transformer inductance $L_{\sigma TF3}$ is taken into account. [10]

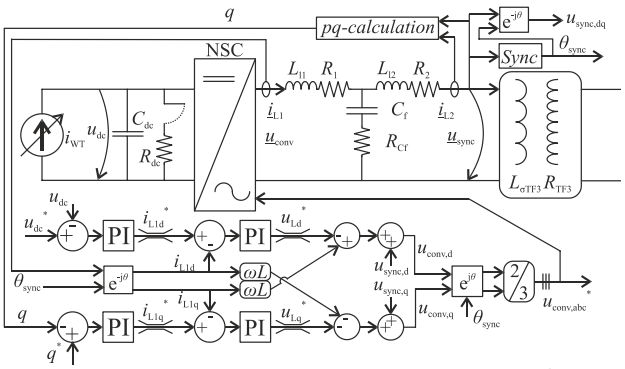

Fig. 6. Wind turbine system model and control system of NSC.

Table I. – LCL-filter and NSC parameters

L_{l1}=300µH	L_{l2}=83µH	R_1=2.4mΩ	R_2=1mΩ	C_f=0.2mΩ
R_{Cf}=0.25Ω	u_{dc}*=1100V	C_{dc}=22mF	R_{dc}=2Ω	

Table II. – Control parameters

Controller	Current	DC-link	Reactive power
Gain	k_i=0.6	k_{udc}=4	k_q=-0.45
Integration time	T_{i_i}=3ms	T_{i_udc}=25ms	T_{i_q}=40ms
Sampling time	T_{s_i}=100µs	T_{s_udc}=100µs	T_{s_q}=100µs
Limitation	$\|u_{Lmax}\|$= 100V	$\|i_{L1dmax}\|$= 900A	$\|i_{L1qmax}\|$= 700A

The used parameter values for the LCL-filter and NSC are shown in Table I. The controller parameters are expressed in Table II. The d- and q-axis current controllers use same parameters. It should be noted that limit values are vector limit values i.e. peak value of the phase quantity.

4. Simulation case

In the simulations two fault points (Fault 1 and Fault 2) are used. It is assumed that the network protection is based on distance protection with the following operation procedure. The three phase fault occurs in point Fault 1 of Fig. 5 at 0.3s. After 200 ms from the beginning of the fault at 0.5s the circuit breaker Cb_{f12} opens and the WT currents flow through strong feeder 2 and through circuit breaker Cb_{f11}. After 300ms from the fault beginning at 0.6s the Cb_{f11} opens and the fault is cleared from the WT viewpoint. [11] When the fault point is Fault 2 same process is applied but circuit breakers Cb_{f21} and Cb_{f22} operates.

The control principle of NSC is chosen such that the reactive power is prioritized during the grid fault. Thus, the reference of NSC current q-component is increased to 591A and the current i_{WT} in (10) is set to zero during the fault.

A. Three-phase fault in feeder 1

The connection point voltages are shown in Fig. 7a. After first transients the converter current waveforms become sinusoidal as shown in Fig. 7b. The transients appear due to the phase angle jump of the grid voltage which is not completely filtered out by the DDSRF-PLL as can be seen from the Fig. 7c, which has different time scaling compared to other Figs. 7 for the sake of clarity. The angular frequency of the PLL shows significant oscillations after the fault as shown in Fig. 7d. However, it takes only 19.5ms for the frequency to settle down within 2 % of the steady state value.

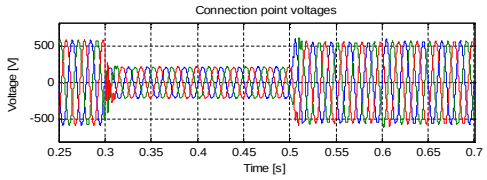

Fig. 7. a) Connection point voltages.

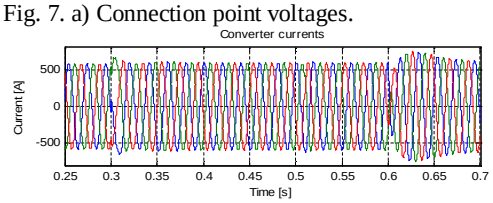

Fig. 7. b) Converter currents.

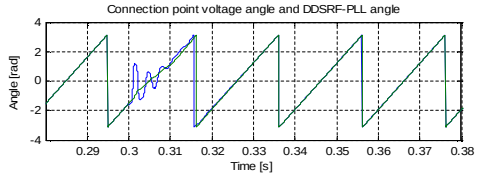

Fig. 7. c) Connection point and DDSRF-PLL angle.

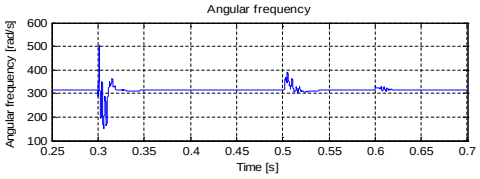

Fig. 7. d) Angular frequency of the DDSRF-PLL.

B. *Three-phase fault in feeder 2*

Next, three-phase fault on the fault point 2 is simulated. The path for fault current is now through feeder 1 which is significantly weaker than the feeder 2. The connection point voltages and converter currents are shown in Fig. 8a and 8b, respectively. It should be noticed that a significant DC-component appears on the converter currents. This is not tolerable because it overstress the network components, especially the WT transformer.

Theoretically, symmetrical voltage dip does not generate a negative sequence component at fundamental frequency. However, the output of the negative sequence component calculated by the decoupling network is not zero during the transients. Thus, the calculated nonzero negative sequence component modifies the value of the calculated positive sequence voltage q-component. If the frequency is not limited the integration part of the PI controller shown in Fig. 8c reaches a high negative value. As a result, the angular frequency of DDSRF-PLL, shown in Fig. 8d, drops near zero. The angle fed to the control system of NSC is the integral of the angular frequency. Thus, the angle shown in Fig. 8e does not change linearly and during near zero angular speed the angle remains nearly constant. Hence, the converter currents contain the DC-component.

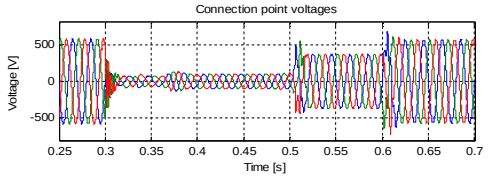

Fig. 8. a) Connection point voltages.

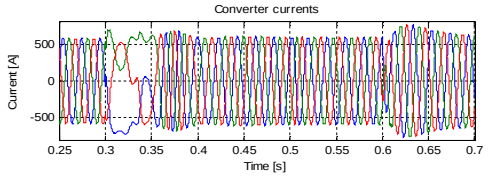

Fig. 8. b) Converter currents.

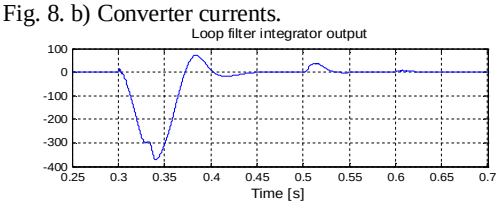

Fig. 8. c) Output of the loop filter integrator.

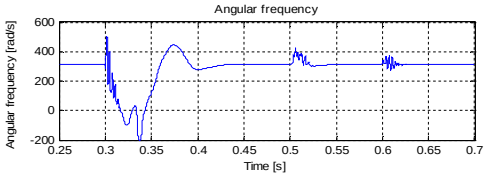

Fig. 8. d) Angular frequency of the DDSRF-PLL.

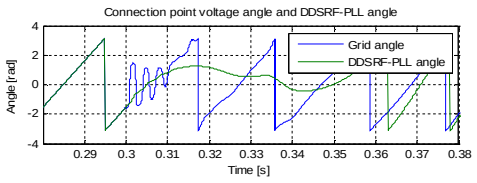

Fig. 8. e) Connection point and DDSRF-PLL angle.

C. *Impact of anti-windup and frequency limitation*

The frequency limitation with integrator anti-windup function of Fig. 4 is added to the DDSRF-PLL loop filter in order to avoid the problems discussed above. The same three-phase fault in feeder 2 is simulated using 5 different frequency limits and 2 different anti-windup time constants. The purpose is to find optimal limits for frequency. The simulation results are collected to the Table III.

The settling time of the first transient is defined as the time measured from the start time of the fault to the time in which the frequency will stay within 2 % of the steady state value. The fundamental frequency negative sequence component and harmonic components from the 2nd to the 20th from the converter current are integrated (summed) in order to measure the quality of the generated current. This harmonic integral is calculated from time span of 0.3-0.7s. The converter currents contain less of harmonics throughout the transient fault when the harmonic integral value is small.

Table III. – Impact of anti-windup and frequency limitation

Frequency limit	**Settling time 2%**	**Harmonic integral**	
	3-phase fault	3-phase fault	2-phase fault
None	0.127s	143.2	75.3
Anti-windup: $T_t = T_i$			
2*pi*(50Hz±3Hz)rad/s	0.092s	87.5	74.3
2*pi*(50Hz±5Hz)rad/s	0.049s	82.6	74.1
2*pi*(50Hz±10Hz)rad/s	0.053s	82.5	74.5
2*pi*(50Hz±15Hz)rad/s	0.057s	82.5	74.7
2*pi*(50Hz±20Hz)rad/s	0.065s	83.6	75.1
Anti-windup: $T_t = T_i/2$			
2*pi*(50Hz±3Hz)rad/s	0.114s	88.7	74.4
2*pi*(50Hz±5Hz)rad/s	0.053s	82.7	74.6
2*pi*(50Hz±10Hz)rad/s	0.054s	83.2	74.9
2*pi*(50Hz±15Hz)rad/s	0.056s	83.4	75
2*pi*(50Hz±20Hz)rad/s	0.063s	84.1	75.1

The simulation results presented in Table III shows that if the frequency limitation is too strict the settling time increases because the frequency limitation decreases the operational range of the loop filter. It should be noted that frequency limits should never be chosen stricter than the detection frequency range of the WT loss of mains protection. Typical frequency limits for loss-of mains protection are around of 50 or 60 (+1…-3)Hz depending on the grid where the WT is connected. [12] The settling time also increases if the frequency limits are set very loose. The amount of undesirable harmonics of the converter current also increases if the limits are set too strict or loose. When 2-phase fault is subjected to the fault point 2, the impact of frequency limitation and anti-windup decreases.

As shown in Table III the response in terms of settling time and current distortion is better when the tracking

time is selected to $T_t=T_i$ instead of $T_t=T_i/2$. Based on the results collected to Table III reasonable selection of frequency limitation is 2*pi*(50Hz±10Hz) rad/s with anti-windup tracking time of $T_t=T_i$.

The same fault as presented in section 4B is now simulated with using above selected frequency limitation and anti-windup tracking time constant. The connection point voltages are shown in Fig. 9a. The integrator anti-windup prevents the integrator output to have a large value as shown in Fig. 9b and the angular speed remains bounded due to the frequency limitation as illustrated in shown in Fig. 9c. Thus, the DDSRF-PLL angle follows the connection point voltage angle with the exception that the phase angle jumps are filtered to a large extent as depicted in Fig. 9d. The converter currents are shown in Fig. 9e and the WT successfully rides through the fault without additional stress to the grid components.

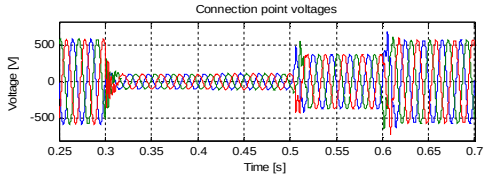

Fig. 9. a) Connection point voltages.

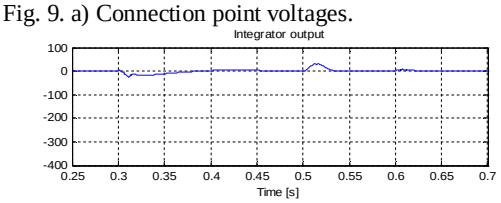

Fig. 9. b) Output of the loop filter integrator.

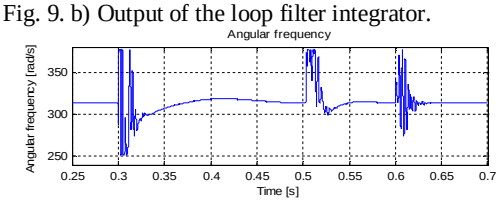

Fig. 9. c) Angular frequency of the DDSRF-PLL.

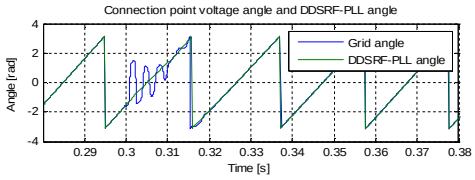

Fig. 9. d) Connection point and DDSRF-PLL angle.

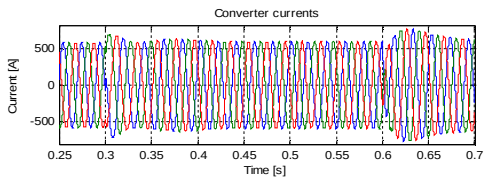

Fig. 9. e) Converter currents.

5. Conclusion

In this paper, the performance of wind turbine synchronizing method DDSRF-PLL during grid fault is studied. The contribution of the paper is to show that if the DDSRF-PLL proposed in many papers is used the control system of NSC may become unstable during a symmetrical grid fault. The instability problem appears only when certain tuning parameters of DDSRF-PLL are used and the fault current path is weak. Thus, the problem may not be detected. This paper proposes that it is mandatory to use PI-controller with integrator anti-windup in the loop filter of DDSRF-PLL. In addition, the impact of angular frequency limitation range on the fault ride through performance is evaluated with comparative simulations.

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