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Smart Grids and Energy Markets

D6.3.3. DEMONSTRATION OF FUNCTIONS FOR MONITORING OF PLC SIGNALS

FINAL REPORT

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1. Introduction

A low cost intelligent electronic device (IED) based on digital signal processor (DSP) and high speed analog-to-digital converter (ADC) is developed for continuous monitoring of power quality and high frequency disturbances in power network. The initial focus of the device is monitoring of power quality and high frequency noises in PLC frequency range. The IED is developed using the hardware architecture presented in Section 2 followed by the software interface presented in Section 3 for post-processing of the signals which is mandatory to draw meaningful results from the captured data.

2. Hardware Architecture

In this section, DSP based hardware architecture of low-cost intelligent electronic device has been discussed. Figure 1 depicts the development approach of IED. The digital board includes signal conditioning, data acquisition and DSP block. Analog signal coming from the LV network needs signal conditioning before an acquisition unit can reliably and accurately acquires the signal. The signal conditioning block includes steps like signal decoupling from the LV network, attenuation, filtering and amplification. Data acquisition block is equipped with 12-bit resolution analog-to-digital converter to sample the analog signal. Afterwards, high-speed DSP will be used to apply signal processing algorithm to mathematically manipulate the digital data.

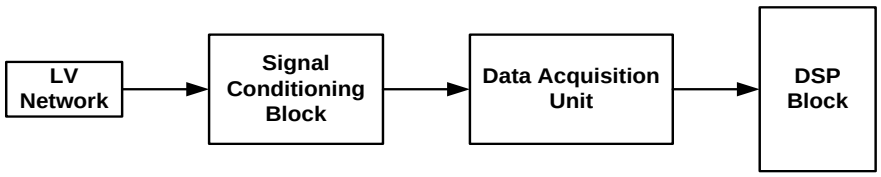

Fig. 1 Development approach of IED

2.1. Digital Signal Processor

The TMS320C6713 DSP Starter Kit (DSK) by Texas Instrument (TI) has been chosen for the development of low-cost and high precision monitoring device. Basic block diagram of TMS320C6713 DSK depicts in Fig. 2. It has a 225 MHz floating-point processor which delivers up to 1350 million floating-point operations per second (MFLOPS), 1800 million instructions per second (MIPS) and with dual fixed-/floating-point multipliers up to 450 million multiply-accumulate operations per second (MMACS). It has L1/L2 memory architecture consisting of a 4K-Bytes of L1P Program

Cache, 4K-Bytes of L1D Data Cache and a L2 memory of 256K-Bytes. It also has 16M-Bytes of SDRAM and 512K-Bytes of non-volatile Flash Memory. The C6713 device is based on the high-performance advance very-long-instruction-word (VLIW) architecture making C6713 DSP an excellent choice for numerically intensive algorithm and real-time signal processing [1].

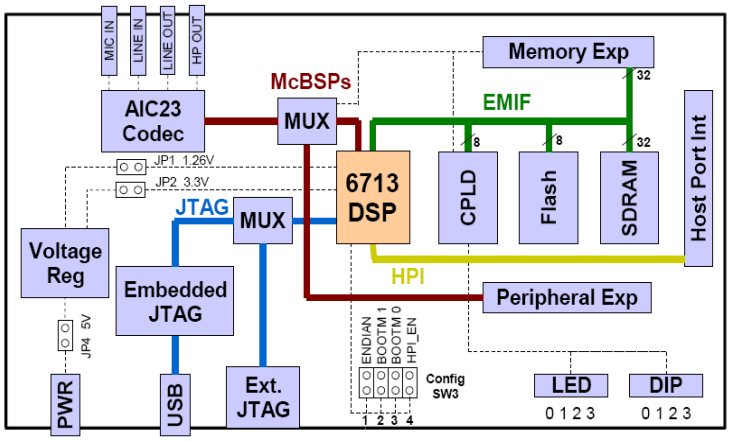

Fig. 2 Basic block diagram of C6713 DSK

2.2. Analog-to-Digital Converter

The ADS7881EVM by TI serves as a reference designed for the prototyping and evaluation of the ADS7881 analog-to-digital-converter. The ADS7881 is a 12-bit 4-MSPS ADC converter with 2.5V internal reference and conversion time of 200ns. The device includes a capacitor based successive approximation register (SAR) ADC converter with inherent sampling and hold. The EVM uses a low noise THS4031 operational amplifier with inverting gain of one and a buffer amplifier. It has high speed parallel interface, onboard signal conditioning and internal reference buffer. To meet the real-time requirement of monitoring device, ADS7881 is an optimal choice for its high

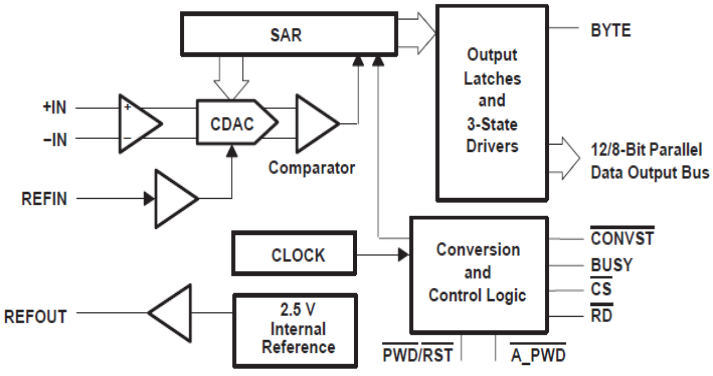

Fig. 3 Basic block diagram of ADS7881 EVM

performance in data acquisition systems. Fig. 3 shows the basic functional block of ADS7881 EVM [2].

2.3. Front-End Circuit

A simple voltage divider circuit as shown in Fig. 4 has been developed as a front-end module for LV network to attenuate the voltage signal to ±2.5 volt. It is the common input voltage range for data acquisition unit.

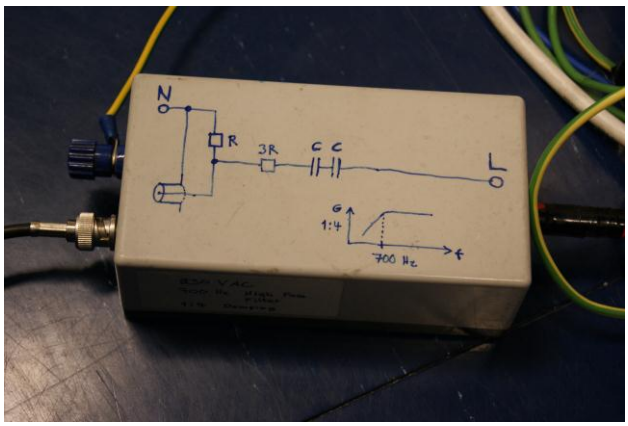

Fig. 4 Front-End module for LV network

2.4. Intelligent Electronic Device Prototype

Finally, the prototype of monitoring equipment following the hardware architecture as explained in section 1.2 has been developed. The data acquisition block has been interfaced with DSP using 5-6K Interface board developed by TI. The prototype IED is shown in Fig. 5. Additional power of ±12 V and +5 V are required to power up the interface board which is necessary for the analog front end and analog power rail of the ADS7881, respectively. The prototype IED enclosed in a box can be seen in Figure 15.

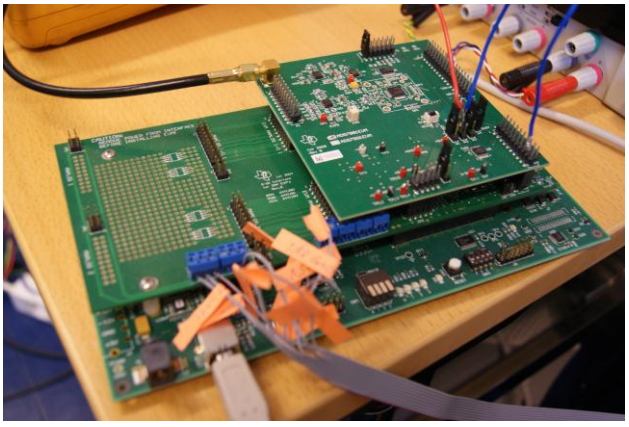

Fig. 5 Prototype of intelligent electronic device

3. Software Interface

The software interface has been developed to collect and process the samples as quickly as possible. Figure 6 depicts the flow diagram of the implementation of the DSP-based equipment. It starts with initializing the necessary functions for board support libraries, DSP and ADC interfaces, resetting interrupt and timer. The most efficient way of accomplishing real-time processing is by using a timer, hardware interrupt and a software interrupt. The algorithm is written to collect 1024 continuous samples then performing additional post processing. As soon as 1024 samples are stored in the Buffer, ADC interrupts the DSP which trigger software interrupt (SWI) and go back to store another set of data to the Buffer. During the time another set of 1024 samples are stored into the Buffer, the SWI executes the inter service routine (ISR) which includes the scaling and signal processing computation of the sampled values. The only time constraint is that all the data inside software interrupt service routine must be processed before the active Buffer fills up, which is much longer than the time between samples. It is much easier to meet the real-time constraints with this implementation.

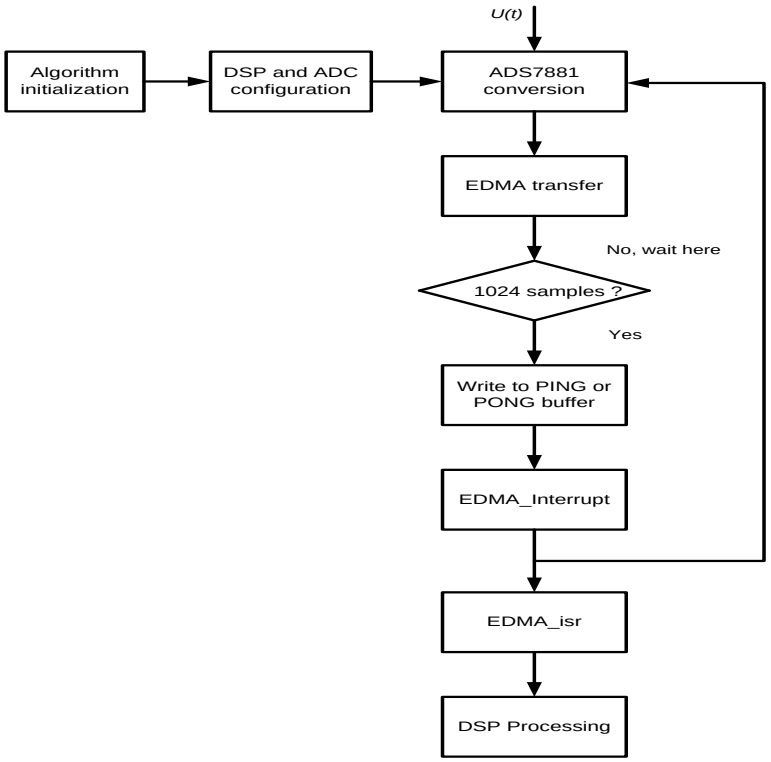

Fig. 6 Flow diagram of the implementation of DSP based monitoring equipment

3.1. Frequency domain analysis

An efficient FFT algorithm that takes very less amount of time comparing to the normal FFT algorithm has been used here to meet the real-time challenges. Typical FFT algorithms assume complex input and output data. Most of the time domain data are real valued. A simple solution to this problem is to pad N-length zero-valued sequence as imaginary component with real-valued signal to make it a complex input. However, this method is obviously inefficient. The algorithm used in this application assumes N-point real sequence as N/2-point complex valued sequence. Let $g(n)$ be an N-point real sequence (N must be even). We want to compute N-point complex FFT using N/2-point FFT computation to reduce the instruction cycle. Complete description of the algorithm can be found in [3].

The following steps are used to accomplish this;

- Form the N/2-point complex valued sequence using N-point real sequence, $x(n) = x_1(n) + jx_2(n)$, where $x_1(n) = g(2n)$ and $x_2(n) = g(2n + 1)$
- Now compute N/2-point complex FFT on the complex valued sequence $x(n)$ to obtain FFT, $X(k) = FFT\{x(n)\}$
- An additional computation is required to get $G(k)$ from $X(k)$

$$G_r(k) = X_r(k)A_r(k) - X_i(k)A_i(k) + X_r(N-k)B_r(k) + X_i(N-k)B_i(k),$$

for $k = 0, 1, \ldots, N/2-1$ and $X(N/2) = X(0)$

$$G_i(k) = X_i(k)A_r(k) + X_r(k)A_i(k) + X_r(N-k)B_i(k) - X_i(N-k)B_r(k)$$

In the above step, only N/2 points of the N-point sequence of $G(k)$ are computed. Since the FFT of a real-sequence has symmetric properties, the remaining N/2 points FFT are easy to compute with the following equations.

$$G_r(N/2) = X_r(0) - X_i(0)$$

$$G_i(N/2) = 0$$

$$G_r(N-k) = G_r(k), \text{ for } k = 1, 2, \ldots, N/2-1$$

$$G_i(N-k) = -G_i(k)$$

$A(k)$ and $B(k)$ in the above equations are sin and cosine coefficient. These values can be computed for N/2 points as follows;

```
A[2 * i]     = 0.5 * (1.0 - sin (2 * PI / (double) (2 * n) * (double)
i));

A[2 * i + 1] = 0.5 * (-1.0 * cos (2 * PI / (double) (2 * n) * (double)
i));

B[2 * i]     = 0.5 * (1.0 + sin (2 * PI / (double) (2 * n) * (double)
i));

B[2 * i + 1] = 0.5 * (1.0 * cos (2 * PI / (double) (2 * n) * (double)
i));
```

3.2. FFT Post Processing

Apart from FFT calculation, the code is also written to calculate minimum, maximum and average value of the FFT spectrum. The frequency range 0 to 150 kHz is divided into 5 bands i.e. 0 to 30 kHz, 30 to 60 kHz, 60 to 90 kHz, 90 to 120 kHz and 120 to 150 kHz. Min, max and average value for each band is being calculated after every 1024 point FFT cycle. Since, limited amount of on-chip memory is a critical problem with DSP. Thus, these calculations help analyzing the noise in different bands without saving the whole FFT spectrum.

4. Experimental Setup

The prototype IED has been tested in the laboratory. A setup using smart energy meter and data concentrator which acts as a central unit has been used. These meters are fully electronic and smart which record the consumption of electric energy and send that information to the utility for billing purposes. They communicate over low voltage network using power line communication. Figure 7 shows the necessary measurement setup to power the signal conditioning, data acquisition and DSP block.

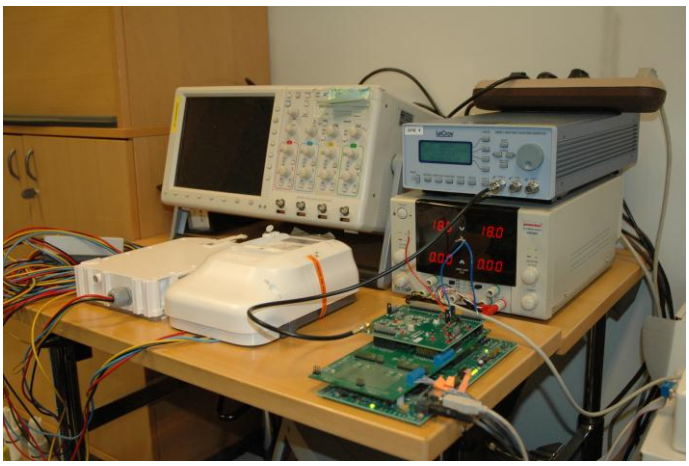

Fig. 7 Measurement setup in laboratory at TUT

Figure 8 shows the smart meter and concentrator setup used to test the PLC communication using prototype IED.

Fig. 8 Smart meter and concentrator setup

Modern energy saving lighting can emit high frequency interference in the frequency range chosen for PLC communication. A low-power load model based on CFL and LED is developed to test the capability of IED to detect the high frequency phenomena in LV network. Figure 9 depicts the load setup consisting of CFL and LED lamps.

Fig. 9 Load model based on CFL and LED lamps built at TUT

A block diagram showing the experimental setup among smart meter, concentrator and load model is shown in Figure 10. Prototype IED is used to monitor the adverse interaction between PLC communication signals and noise generated by the load.

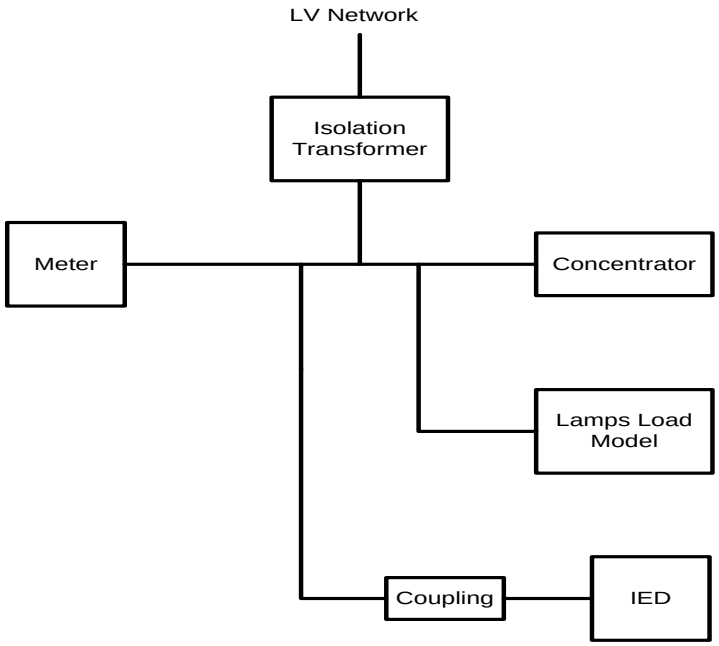

Fig. 10 Load connected to experimental setup along with meter and concentrator

5. Results

This section explains the results captured by prototype IED. Matlab has been used to plot all the figures for better presentation and image quality. Before making any measurements with the laboratory setup, a reliability test to see the performance of IED has been conducted. FFT spectrum of 80 kHz signal is computed by the IED and measured by Rhode & Schwarz spectrum analyzer ESPI-3. Figure 11 shows the comparison between the results produced by IED and spectrum analyzer.

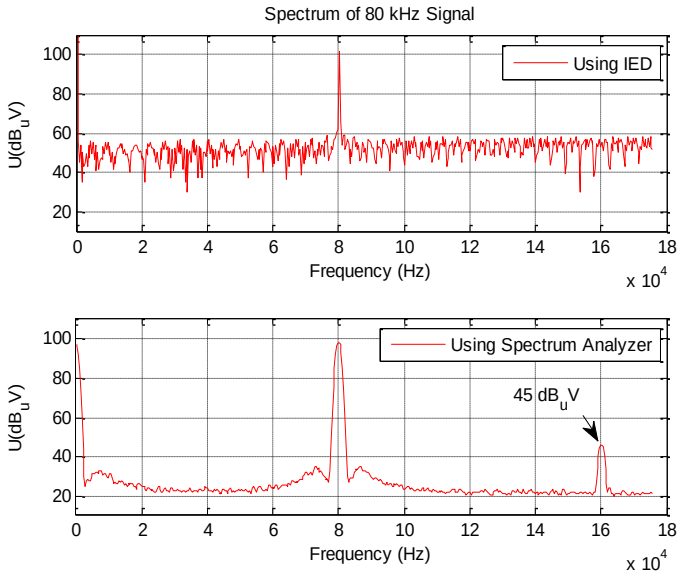

Figure 11. Spectrum analysis using IED and spectrum analyzer

Spectrum analyzers are normally expensive measurement equipment comparing to the low cost IED. Despite the low sampling frequency and dynamic range, IED has computed the spectrum of 80 kHz signal quite accurately comparing to the result produced by spectrum analyzer. Thus, it shows very good performance of the IED.

Now IED is connected with the load setup to monitor the behavior of PLC network. Figure 12 depicts the time-domain waveform (without scaling) of 50 Hz signal captured by prototype IED. It is clearly visible that PLC signals are modulated over 50 Hz cycle and communication between meter and concentrator is going on in most of the cycle. No communication is going on between meter and concentrator for a short duration of time which is indicated in the figure.

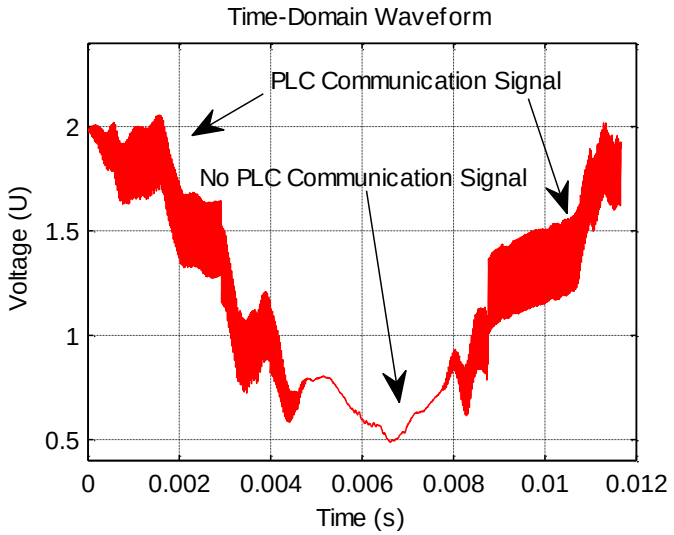

Fig. 12 Time-domain waveform captured by the IED

Frequency-domain analysis gives a description of the distribution of the energy in the signal as a function of frequency. It is necessary to determine other high frequency components which act as a noise in PLC communication. Figure 13 and Figure 14 the frequency domain spectrum of waveform acquired by IED. It is evident from both the graph that high frequency noises caused by load model and probably due to other power electronic devices attached to the distribution network are clearly present. It can also be noticed from the spectrum that IED is capable of monitoring frequencies up to approximately 175 kHz which covers the whole PLC frequency range.

The IED has been designed to meet the EMC standard EN 55011 which limits the emission from RF equipment to be below 56 dBµV at 150 kHz and decrease to 46

dBµV at 500 kHz. Noise floor of the IED is around 45 dBµV which can be observed from Figure 13. It can be further analyzed from Figure 11 that spectrum measured by spectrum analyzer has second harmonic at 160 kHz which is not found in the spectrum computed by IED because its amplitude is just below the noise floor of the IED.

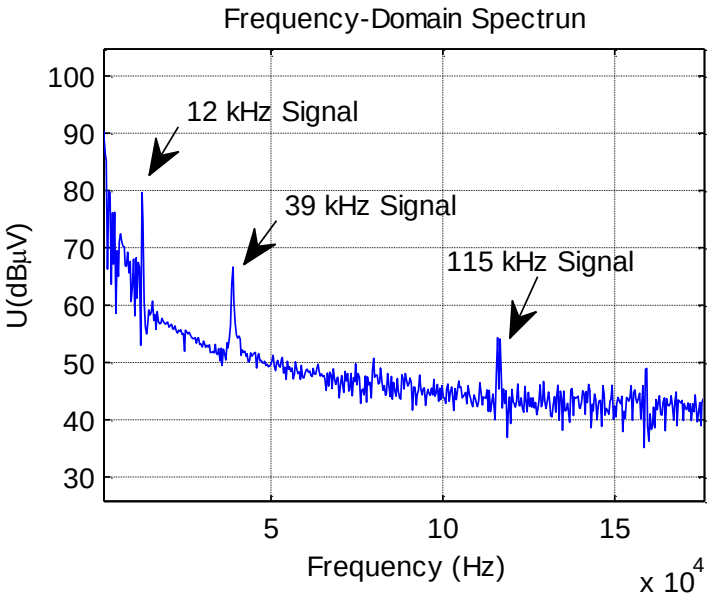

Fig. 13 Frequency-domain spectrum computed by the IED

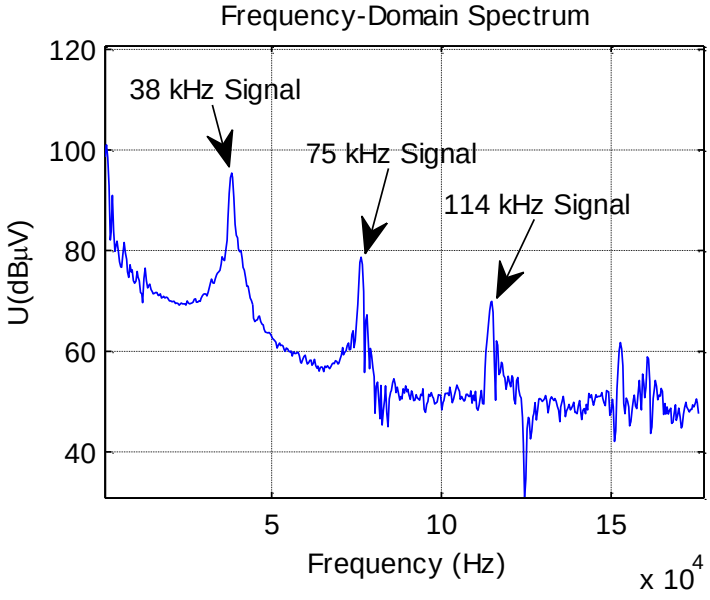

Fig. 14 Frequency-domain spectrum computed by the IED

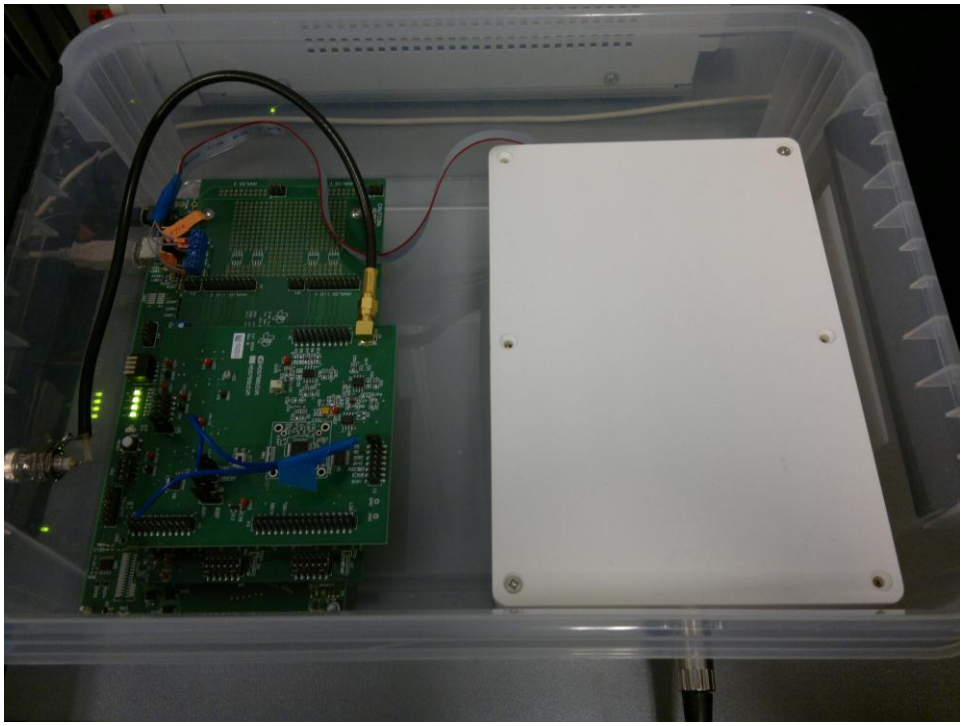

Fig. 15 Final prototype of the IED enclosed in a box with additional power supply needed for ADC and interface board.

6. Conclusion

The prototype IED has been tested in the laboratory with adequate equipment. The test results have shown that the IED is fully capable of monitoring the whole PLC frequency range. It has shown very efficient performance in the robust distribution network and computed very accurate results.

The future prospect of the IED is to make an algorithm to extract the valuable information from the captured data to classify the quality the signal. The algorithm will be tested by installing the IED in different locations permanently to monitor the time-variant behavior of the LV network over longer periods of time.

References

[1] User guide, TMS320C6713 floating-point digital signal processor, SPRS186L, Texas Instrument, USA, 2005.

[2] User guide, ADS7881 evaluation module, SLAU150, Texas instrument, USA, 2004.

[3] Efficient FFT Computation of Real Input, Texas Instrument.
<http://processors.wiki.ti.com/index.php/Efficient_FFT_Computation_of_Real_Input.>